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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/708,490	11/09/2000	Chie Iwasa	03180.0269	1827

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EXAMINER	
LAU, TUNG S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/708,490	IWASA, CHIE	
	Examin r	Art Unit	
	Tung S Lau	2863	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 9, 13, 16, 19, 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Vu et al. (U.S. Patent 6,140,832).

Regarding claim 1:

Vu discloses a semiconductor testing apparatus for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples (abstract), but returned from a user to a manufacture as faulty samples so as to improve testing performance (Col. 1, Lines 5-9) , the semiconductor testing apparatus comprising an IDDQ measuring circuit configured to measurement current data of good and returned samples (Col. 1-2, Lines 40-25), by supplying test vector data to the good and returned samples; a determination circuit configured to determined range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data wherein the IDDQ measuring circuit tests the

target semiconductor devices by applying the test vector data for the effective address pairs (Col. 1-2, Lines 40-25, (Col. 3, Lines 43-63).

Regarding claim 5:

Vu discloses a semiconductor testing method for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples (Col. 1, Lines 5-20), but returned from a user to a manufacture as faulty samples so as to improve testing performance, the method comprising reading test vector data (Col. 1-2, Lines 40-25), measuring current data of good samples and returned samples by supplying the test vector data to the good and retuned samples (Col. 1-2, Lines 40-25); determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data (Col. 1-2, Lines 40-25, Col. 1, Lines 5-33); and applying the test [vectors of] vector data for the effective address pairs to the target semiconductor devices for testing (Col. 1-2, Lines 40-25).

Regarding claim 9:

Vu discloses a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, an IDDQ measuring circuit configured to test semiconductor devices by applying an effective test vector data, configured to feed back data of returned samples which have been shipped as good samples, returned from a user to a manufacture as faulty samples so as to improve testing

performance, the program comprising instructions configured to read measurement data (Col. 1-2, Lines 39-25), instructions configured to supply the test vector data to good samples and returned samples (Col. 1-2, Lines 39-25, Col. 1, Lines 5-33); instructions configured to measure current data of the good and returned samples (Col. 1-2, Lines 39-25); instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data; and instructions configured to apply the test vector data for the effective address pairs for testing (Col. 1-2, Lines 5-25).

Regarding claim 13:

Vu discloses a program a semiconductor testing method of specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples but returned from a user to a manufacture as faulty samples so as to improve testing performance (abstract), the method comprising reading a test program and test vector data supplying the test vector data to good and returned samples (Col. 1-2, Lines 40-25), measuring current data of the good and returned samples (Col. 1-2, Lines 40-25), employing an IDDQ measuring circuit; determining a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured current data (Col. 1-2, Lines 40-25, Col. 1, Lines 5-33); applying the test vector data for the effective address

pairs and specifying a faulty part within the target semiconductor device by measuring an emission from the target semiconductor device (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64).

Regarding claim 16:

Vu discloses a semiconductor testing apparatus for specifying a faulty part in a semiconductor device, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the apparatus comprising a read circuit configured to read test vector data and a test program (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64); an IDDQ measuring circuit configured to measure current data includes a test program (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64), test vector data, data] of good samples and returned samples, determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process; and a faulty part specifying circuit configured to apply the test vector data for the effective address pairs to the target semiconductor device and to specify a faulty part by measuring an emission from the target semiconductor device (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64).

Regarding claim 19:

Vu discloses a program with which a semiconductor testing method is executed by a computer in a semiconductor testing apparatus which comprises a read circuit, a determination circuit, and a faulty part specifying circuit, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a manufacture as faulty samples so as to improve testing performance, the program comprising instructions configured to read a test program and test vector data instruction configured to measures current data of good samples and return samples by employinq an IDDQ measuring circuit (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64), by supplying the test vector data to good returned samples; instructions configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices in a manufacturing process based upon the measured data (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64); instructions to apply the test vector data for the effective address pairs to the target semiconductor device; and instructions to specify a faulty part within the target semiconductor device by measuring an emission from the tar et semiconductor device (Col. 1-2, Lines 40-25, Col. 3, Lines 42-64).

Regarding claims 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 17 and 18:

Vu discloses a semiconductor testing method, program, apparatus for specifying a faulty part in a semiconductor device, including the rate of change in current value of the device (fig. 4), acquire effective address pair (fig. 4, col. 3, lines 44-

55), display rate falling outside of the range of pass/fail decision criteria (col. 2, lines 1-25), measure current value for pass fail comparison (col. 2, lines 1-25, Col. 3, Lines 44-63), displaying result (fig. 2, 3, 4).

Response to Arguments

2. Applicant's arguments filed 7/18/2003 have been fully considered but they are not persuasive.

A. Applicant argues that the prior art does not show the " semiconductor testing apparatus for testing and configured to feedback data of returned samples which have been shipped as good samples, but returned from a users to manufacture as faulty samples"; Vu discloses the "semiconductor testing apparatus for testing and configured to feedback data of returned samples which have been shipped as good samples, but returned from a users to manufacture as faulty samples" in Col. 1-2, Lines 5-25.

B. Applicant argues that the prior art does not show "an IDDQ measuring circuit configured to measure current data of good samples and the returned samples by supplying test vector data to the good and returned samples and determination circuit configured to determined a range of pass/fail decision and effective address pairs for testing target semiconductors device based upon the current data"; Vu discloses show "an IDDQ measuring circuit configured to measure current data of good samples and the returned samples by supplying

test vector data to the good and returned samples and determination circuit configured to determined a range of pass/fail decision and effective address pairs for testing target semiconductors device based upon the current data" in Col. 1-2, Lines 40-25, Col. 3, Lines 42-63, fig. 3, 4.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung S Lau whose telephone number is 703-305-3309. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 703-308-3126. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-5841 for regular communications and 703-308-5841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TC2800 RightFAX Telephone Numbers : TC2800 Official Before-Final RightFAX - (703) 872-9318, TC2800 Official After-Final RightFAX - (703) 872-9319

TC2800 Customer Service RightFAX - (703) 872-9317

TL August 25, 2003

John Barlow
Supervisory Patent Examiner
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